Confirmation No. 7347

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	SHRIVASTAVA, *et al.*	Examiner:	Knoll, C.
Serial No.:	10/566,515	Group Art Unit:	2111
Filed:	January 30, 2006	Docket No.:	US030254US2
Title:	MICROCONTROLLER WITH AN INTERRUPT STRUCTURE HAVING PROGRAMMABLE PRIORITY LEVELS WITH EACH PRIORITY LEVEL ASSOCIATED WITH A DIFFERENT REGISTER SET		

APPEAL BRIEF

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Dear Sir:

This revised Appeal Brief is presented in response to the Notification of Non-Compliant Appeal Brief mailed May 5, 2008, and is submitted pursuant to 37 C.F.R. §41.37, in support of the Notice of Appeal filed February 29, 2008 and in response to the rejections of claims 1-21 as set forth in the Final Office Action dated November 29, 2007, and in acknowledgment of the Advisory Action dated February 27, 2008.

Appellant submits that the previous Brief filed April 28, 2008 was fully compliant in that the "Summary of the Claimed Subject Matter Section" properly included page and line number references to the Specification, along with paragraph numbers for convenience. The inclusion of paragraph numbers in addition to page and line numbers should not render a brief non-compliant. Appellant is unaware of a brief being deemed non-compliant on such grounds. As such, the Notification of Non-Compliance should be removed, and the Brief as originally filed should be considered. Nevertheless, to facilitate consideration of this appeal at the earliest possible date, Appellant submits this revised Appeal Brief.

Appellant believes that no fee is due. However, authorization to charge/credit **Deposit Account number 50-0996 (NXPS.281PA)** is hereby given in case there are additional fees/overages in support of this filing.

I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 017529/0075 to Koninklijke Philips Electronics, N.V., headquartered in Eindhoven, the Netherlands. We have been authorized by both the assignee of record and NXP Semiconductors to convey herein that the entire right, title and interest of the instant patent application has been transferred to NXP Semiconductors.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1-21 stand rejected and are presented for appeal. A complete listing of the claims under appeal is provided in an Appendix to this Brief.

IV. Status of Amendments

No amendments have been filed subsequent to the Office Action dated November 29, 2007.

V. Summary of Claimed Subject Matter

Appellant's recited invention relates to systems and methods, and to storage media for use therein, that implement an interrupt structure having programmed priority levels, each priority level being associated with a different register set.

Commensurate with independent claim 1, an example embodiment of the present invention is directed to a system that includes a processor (*see, e.g.*, processor 180 shown in Fig. 1, page 4:8-17) that executes logical or arithmetic operations (*see, e.g.*, page 1:10-24), a plurality of register bank blocks (*see, e.g.*, register bank blocks 120, 121, 122, 123, 124 and 125 shown in Fig. 2, page 7:20 to page 8:18) used as special function registers by the processor during the execution of the logical or arithmetic operations (*see, e.g.*, special

function register block 501 shown in Fig. 5, page 8:28 to page 9:3), and a register bank block decoder circuit (*see, e.g.*, decoder circuit 140 shown in Fig. 2 and 701 shown in Fig. 7, page 11:3-14) for activating one and only one of the plurality of register bank blocks (*see, e.g.*, page 2:13-18), the register bank block decoder circuit responsive to interrupt event operations for selecting the one of the plurality of register bank blocks for being activated (*see, e.g.* page 2:13-18 and page 11:3-14), where different interrupt event operations result in selection of different ones of the plurality of register bank blocks (*see, e.g.*, page 2:13-18 and page 11:3-14).

Commensurate with independent claim 13, an example embodiment of the present invention is directed to a method of switching processing resources in a data processing system, which includes the steps of providing a plurality of register bank blocks (*see, e.g.*, register bank blocks 120, 121, 122, 123, 124 and 125 shown in Fig. 2, page 7:20 to page 8:18), utilizing a first register bank block from the plurality of register bank blocks as special function registers during execution of logical or arithmetic operations (*see, e.g.*, special function register block 501 shown in Fig. 5, page 8:28 to page 9:3), receiving of an interrupt request for initiating an interrupt event (*see, e.g.*, page 2:19-27 and page 11:3-14), determining if the interrupt request is to be fulfilled (*see, e.g.*, page 2:19-27), and if so, selecting a second register bank block from the plurality of register bank blocks (*see, e.g.*, page 2:19-27 and page 11:3-14), the selected second register bank block in isolation from the first register bank block (*see, e.g.*, page 2:19-27), and utilizing the second register bank block from the plurality of register bank blocks as special function registers during execution of logical or arithmetic operations (*see, e.g.*, page 2:19-27 and page 11:3-14).

Commensurate with independent claim 13, an example embodiment of the present invention is directed to a storage medium (*see, e.g.*, page 3:1-8) having data stored thereon, the data for implementation of a processing system that includes first instruction data (*see, e.g.*, page 3:1-8 and page 7:20-25) for providing a plurality of register bank blocks that are used as special function registers during execution of logical or arithmetic operations (*see, e.g.*, special function register block 501 shown in Fig. 5, page 8:28 to page 9:3), and second instruction data (*see, e.g.*, page 3:1-8 and page 7:30-35) for providing a register bank block decoder circuit for activating one of the plurality of register bank blocks in isolation (*see,*

e.g., page 3:1-8), the register bank block decoder circuit responsive to interrupt event operations for selecting the one of the plurality of register bank blocks for being activated (*see, e.g.*, page 3:1-8 and page 11:3-14), where different interrupt event operations result in selection of different ones of the plurality of register bank blocks (*see, e.g.*, page 3:1-8 and page 11:3-14).

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and their legal equivalents for a complete statement of the invention.

VI. Grounds of Rejection to be Reviewed Upon Appeal

A. Claims 1-7, 11, 13-16 and 19-21 stand rejected under 35 U.S.C. § 103(a) over Mitsuhira (U.S. Patent No. 5,155,583) in view of Yoshida (U.S. Patent No. 5,450,566).

B. Claims 8-10 and 17-18 stand rejected under 35 U.S.C. § 103(a) over Mitsuhira (U.S. Patent No. 5,155,583) in view of standard register use, and in further view of Fujimura (U.S. Patent No. 5,751,988).

C. Claim 12 stands rejected under 35 U.S.C. § 103(a) over Mitsuhira (U.S. Patent No. 5,155,583) in view of standard register use, and in further view of Hohl (U.S. Patent No. 6,035,422).

VII. Argument

As set forth below, Appellant submits that the claimed invention is allowable over the cited references because the obviousness rejections are based on art that teaches away from, and that fails to provide correspondence to, the claimed invention. In particular, the cited references do not disclose the use of special function registers, and the use of special function registers is contrary to the teachings of the primary Mitsuhira reference used in each of the rejections.

A purported obviousness rejection based on a combination of references fails unless the references are properly combinable and teach or suggest all the recited claim elements. Without a reasonable expectation of success and a valid reason for combining, references are not properly combinable. These conditions cannot be satisfied when a reference teaches away from the proposed combination or modification, or a reference is rendered inoperable for its intended purpose upon making the proposed combination or modification. Appellant submits that the Examiner's obviousness rejections fail to meet the required criteria. Appellant further submits that the Examiner's rejections are predicated on conjecture and opinion without proper analysis of correspondence between the cited art and the features of the claims, without properly articulating how the proposed combinations would be made, and without fully addressing the substance of Appellant's arguments. Appellant therefore requests that the Board reverse the rejections.

A. The § 103(A) Rejection Of Claims 1-7, 11, 13-16 And 19-21 Over Mitsuhira In View Of Yoshida Is Improper And Should Be Reversed.

1. The proposed combination does not correspond to all the features of the claims.

Appellant respectfully submits that the cited portions of the Mitsuhira reference, taken alone or in view of Yoshida, do not correspond to the claimed invention. For example, the Mitsuhira reference does not teach or suggest the use of special function registers in the manner recited in the claimed invention. Mitsuhira discloses a data memory (36) that includes banks of general registers (*see, e.g.*, Mitsuhira's Figure 1; Col. 4:15-21). Nowhere does Mitsuhira disclose or suggest the use of special function registers in place of the general registers. Moreover, Yoshida includes no disclosure of special function registers, and thus does not cure the deficiency of Mitsuhira (Appellant notes that Yoshida is cited only for allegedly disclosing performance of arithmetic operations on register data, and was not asserted in the Final Office Action for disclosing special function registers).

As Appellant demonstrated in the response of September 7, 2007, special function registers, as known to those of skill in the art and as consistent with Appellant's Specification, are accessed by a processor as if they were internal memory. *See, e.g.,* U.S. Patent No. 5,734,857 in the Summary of the Invention section, and the printout from **http://www.hobbyprojects.com/8051_tutorial/special_function_registers.html** (which was attached in Appellant's September 7, 2007 response, and is re-attached hereto for convenience). In contrast, the memory 36 disclosed by Mitsuhira is used to temporarily store a copy of data from program status word (PSW) 20 and program counter 18. The temporarily stored data is then restored to PSW 20 and PC 18 rather than accessed as internal memory. As such, Mitsuhira's description of the use of the registers within memory 36 is consistent with the term "general register" as used by Mitsuhira, and is inconsistent with the term "special function register" as used by Appellant and as understood in the art.

An object of certain embodiments of Appellant's invention is to facilitate the execution of an interrupting program stream without storing and restoring interrupted program stream critical data (*see, e.g.,* Appellant's Specification, Paragraph 0005), whereas the cited portions of Mitsuhira teach storing and restoring critical data in response to interrupt requests. The cited portions of the Mitsuhira reference teach that, in response to an interrupt signal, CPU 16 operates to save the contents of PC 18 and PSW 20 in the selected register bank (*i.e.,* register banks 1, 2 and 3 of data memory 36). *See, e.g.,* Mitsuhira Figures 1 and 2; Col. 6:3-12. The register banks taught by Mitsuhira are used to store data while interrupt requests are processed by the CPU 16. Mitsuhira's resister banks are not used as special function registers by CPU 16 during the execution of logical or arithmetic operations as recited in the claimed invention.

In the Advisory Action, the Examiner responds to Appellant's arguments that the proposed combination fails to teach special function registers by stating that Yoshida uses registers to perform what the Examiner deems to be "special functions." The passage of Yoshida cited for support (*i.e.*, Yoshida Col. 4:45-48) merely discloses an instruction to add the contents of two registers and store the result in a third register. The Examiner makes the conclusory statement that such disclosure adequately sets forth special function registers, without providing any documentary evidence to support such an opinion. In particular, the Examiner has not addressed Appellant's explanation of special function registers as set forth above and in previous responses, much less provided any basis for how the registers disclosed in either Mitsuhira or Yoshida might conform thereto. Appellant further submits that the Examiner's failure to provide a full explanation is contrary to M.P.E.P. § 707.07(f) which states, "[i]n order to provide a complete application file history and to enhance the clarity of the prosecution history record, an examiner must provide clear explanations of all actions taken by the examiner during prosecution of an application."

For these reasons, the proposed combination of Mitsuhira in view of Yoshida cannot be properly read as disclosing the use of special function registers as claimed by Appellant. Therefore, Appellant submits that the § 103(a) rejection is improper and should be reversed.

2. No valid reason has been presented for modifying Mitsuhira in the proposed manner.

Appellant respectfully submits that no valid reason has been presented for combining Mitsuhira with Yoshida in a manner that would result in Appellant's invention. The Examiner admits that Mitsuhira fails to disclose the use of registers for special functions, but argues that one of skill in the art would modify Mitsuhira in view of Yoshida's alleged disclosure of registers that have particular functions during the execution of arithmetic operations. The only rationale provided by the Examiner in support of modifying Mitsuhira in such a manner is that it "allows for enhancements, such as efficient use of register addressing modes." *See* Final Office Action, page 2.

As an initial matter, Appellant has been unable to ascertain what the Examiner's alleged modification of Mitsuhira involves, and has requested clarification. For instance, to the extent that Yoshida discloses register data is being used in arithmetic operations, the Examiner has not provided information explaining what registers are being referenced, where the arithmetic operations are to be implemented, or how efficient use of register addressing modes would be seen as a result of any combination.

Appellant further submits that the § 103(a) rejection fails because the Examiner's asserted modification undermines the operation of the Mitsuhira reference. As indicated in M.P.E.P. § 2143.01, when the asserted modification would undermine both the operation and the purpose of the main reference, the §103 rejection is improper. *See also In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984) (A §103 rejection cannot be maintained when the asserted modification undermines the operation and/or purpose of main reference.). As Appellant noted above, Mitsuhira discloses that the register banks are used in a manner that is inconsistent with the use of special function registers. As such, to the extent that the Examiner views Yoshida's register functions as "special," any modification to convert Mitsuhira's registers into special function registers would alter Mitsuhira's disclosed mode of operation.

Therefore, Appellant submits that no valid reason to modify the Mitsuhira reference using the teachings of Yoshida has been presented. Therefore, Appellant submits that the § 103(a) rejection is improper and should be reversed.

B. The § 103(A) Rejection Of Claims 8-10 And 17-18 Over Mitsuhira In View Of Standard Register Use (As Applied Above), And In Further View Of Fujimura Is Improper And Should Be Reversed.

Appellant respectfully submits that the § 103(a) rejection of claims 8-10 and 17-18 is improper for at least the reason that it is based on the improper combination of Mitsuhira and Yoshida, discussed in Section A above, and that the Fujimura reference appears to provide no teaching or disclosure to cure the noted underlying deficiencies of Mitsuhira and Yoshida.

Fujimura is cited for its alleged disclosure of returning from an interrupt and restoring existing conditions, which the Examiner admits the underlying references fail to teach. However, the Examiner has made no effort to analyze how the elements purportedly taught by Fujimura are to be combined with Mitsuhira and Yoshida. For example, it is unclear how the combination of references would correspond to the feature recited in claim 8 directed to register bank block selection data indicative of a pre interrupt switch state. As another example, neither the Examiner (nor the applied references) clearly indicate what would correspond to a pre interrupt register bank block selection signal derived from the stored register bank block selection data, as recited in claim 8. Appellant submits that the Examiner has failed to provide support for: 1) what aspects of the Fujimura reference correspond to the various claim recitations; and 2) how these aspects would function in the asserted circuit of the Mitsuhira reference. Without a showing of correspondence for each claim limitation and an analysis of the limitations as a whole, Appellant submits that the rejections cannot stand.

For at least these reasons, Appellant submits that the § 103(a) rejection of claims 8-10 and 17-18 is improper and should be reversed.

C. The § 103(A) Rejection Of Claim 12 Over Mitsuhira In View Of Standard Register Use (As Applied Above), And In Further View Of Hohl Is Improper And Should Be Reversed.

Appellant respectfully submits that the § 103(a) rejection of claim 12 is improper for at least the reason that it is based on the improper combination of Mitsuhira and Yoshida, discussed in Section A above, and that the Hohl reference appears to provide no teaching or disclosure to cure the noted underlying deficiencies of Mitsuhira and Yoshida.

Hohl is cited for its alleged disclosure of accessing register data during debugging, which the Examiner admits the underlying references fail to teach. However, as with the other § 103(a) rejections discussed above, the Examiner has made no effort to analyze how the elements purportedly taught by Hohl are to be combined with Mitsuhira and Yoshida in a way that would result in the claimed invention. Appellant submits that the Examiner has failed to provide support for: 1) what aspects of the Hohl reference correspond to the various claim recitations; and 2) how these aspects would function in the asserted circuit of the Mitsuhira reference. Without a showing of correspondence for each claim limitation and an analysis of the limitations as a whole, Appellant submits that the rejections cannot stand.

For at least these reasons, Appellant submits that the § 103(a) rejection of claim 12 is improper and should be reversed.

VIII. Conclusion

In view of the above, Appellant submits that the rejections of claims 1-21 are improper. Appellant therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application. Authority to charge the undersigned's deposit account was provided on the first page of this brief.

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APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 10/566,515)

1. A system comprising:

a processor that executes logical or arithmetic operations;

a plurality of register bank blocks used as special function registers by the processor during the execution of the logical or arithmetic operations and,

a register bank block decoder circuit for activating one and only one of the plurality of register bank blocks, the register bank block decoder circuit responsive to interrupt event operations for selecting the one of the plurality of register bank blocks for being activated, where different interrupt event operations result in selection of different ones of the plurality of register bank blocks.

2. A system according to claim 1, further comprising:

a memory circuit for storing of a first program stream and for storing of a second program stream, wherein the processor utilizes a first register bank block from the plurality of register bank blocks during execution of the first program stream, and upon the occurrence of an interrupt resulting from an interrupt event associated with the second program stream, the processor executes the second program stream utilizing a second register bank block, the second register bank block different and logically isolated from the first register bank block.

3. A system according to claim 2, wherein the second program stream has a higher interrupt priority than the first program stream.

4. A system according to claim 1, further comprising:

an input data bus and,

an input switching circuit coupled to the plurality of register bank blocks and having a selection input port for receiving a register bank block selection signal from the register bank block decoder circuit, the input switching circuit for activating one of the plurality of register

bank blocks in dependence upon the register bank block selection signal, the activated one of the plurality of register bank blocks being coupled to the input data bus.

5. A system according to claim 4, wherein the input switching circuit is a multiplexer circuit.

6. A system according to claim 4, further comprising:

an output data bus; and,

an output switching circuit coupled to the plurality of register bank blocks and having a selection input port for receiving the register bank block selection signal from the register bank block decoder circuit, the output switching circuit for switchably coupling the activated one of the plurality of register bank blocks to the output data bus.

7. A system according to claim 6, wherein the output switching circuit is a multiplexer circuit.

8. A system according to claim 6, further comprising a circuit for storing and retrieving of register bank block selection data derived from the register bank block selection signal, the register bank block selection data indicative of a pre interrupt switch state, wherein upon terminating of an interrupt event, the input switching circuit and the output switching circuit are provided with a pre interrupt register bank block selection signal derived from the stored register bank block selection data.

9. A system according to claim 8, wherein the state of the circuit for storing and retrieving of the register bank block selection data is based on interrupt priority.

10. A system according to claim 6, wherein the register bank block selection signal is based solely on interrupt priority.

11. A system according to claim 1, wherein a first register bank block from the plurality of register bank blocks is concurrently enabled along with a second different register bank block from the plurality of register bank blocks, the second different register bank block independently addressable from the first register bank block.

12. A system according to claim 1, further comprising a debug bank select register coupled to the register bank block decoder circuit, the debug bank select register for providing access to program stream data stored within the plurality of register bank blocks during a step of debugging.

13. A method of switching processing resources in a data processing system comprising the steps of:

providing a plurality of register bank blocks;

utilizing a first register bank block from the plurality of register bank blocks as special function registers during execution of logical or arithmetic operations;

receiving of an interrupt request for initiating an interrupt event;

determining if the interrupt request is to be fulfilled, and if so, then: selecting a second register bank block from the plurality of register bank blocks, the selected second register bank block in isolation from the first register bank block; and,

utilizing the second register bank block from the plurality of register bank blocks as special function registers during execution of logical or arithmetic operations.

14. A method according to claim 13, wherein a first program stream is provided for utilizing of the first register bank block and a second program stream is provided for utilizing the second register bank block.

15. A method according to claim 14, wherein the first program stream has a lower interrupt priority than the second program stream, the interrupt priority used in the step of determining whether to fulfill the interrupt request.

16. A method according to claim 14, wherein a processor executes the first and second program streams.

17. A method according to claim 16, further comprising the steps of:
halting execution of the second program stream;
selecting the first register bank block; and,
resuming execution of the first program stream.

18. A method according to claim 17, wherein executing the instructions of the second program stream takes place without altering the contents of the first register bank block in suspended use by the first program stream.

19. A method according to claim 14, further comprising the step of:
providing a memory circuit having a first memory region for storing of program stream data related to the first program stream.

20. A method according to claim 14, wherein the first and second program streams have stored therein instruction data for storing and restoring of register bank block contents.

21. A storage medium having data stored thereon, the data for implementation of a processing system comprising:
first instruction data for providing a plurality of register bank blocks that are used as special function registers during execution of logical or arithmetic operations and,
second instruction data for providing a register bank block decoder circuit for activating one of the plurality of register bank blocks in isolation, the register bank block decoder circuit responsive to interrupt event operations for selecting the one of the plurality of register bank blocks for being activated, where different interrupt event operations result in selection of different ones of the plurality of register bank blocks.

APPENDIX OF EVIDENCE

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.